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METHOD OF FABRICATING INDUCTOR AND STRUCTURE FORMED THEREFROM

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a method of fabricating a semiconductor device and a structure formed therefrom, and more particularly to a method of fabricating an inductor and a structure formed therefrom.

Description of the Related Art

[0002] In integrated circuits, inductors are very important devices. The inductors are usually circular or rectangular spiral metal wires and widely used in different applications. For high-frequency devices, they require high performance of inductors which means that they have high quality factors. For example, in wireless communication, the quality factor (Q) of inductors should have about 60. The definition of quality factor is represented by the following formula:

$$Q = \omega_0 L/R \qquad (1)$$

[0003] Wherein ω_0 is the resonant angular frequency of the inductor, R is the resistance of the inductor and L is the inductance of the inductor.

[0004] From formula (a), when L is fixed, quality value will increase with respect to the increase of the resonant angular frequency or the decrease of the resistance, wherein the resistance is proportional to the square of the current density. Therefore, one method of enhancing the quality factor is to increase the cross-sectional

area of the metal wires for reducing the current density therein. The method can reduce the resistance of the metal wires and increase the quality factor.

[0005] Therefore, in semiconductor devices the high quality factor can be achieved by increasing the width of the metal lines. However, if the width of the metal lines is too large, charges will accumulate at the corners of the metal lines and the current density therefore cannot be reduced. Accordingly, the quality factor of the inductor cannot be enhanced. Therefore, the quality factor generated from the prior art semiconductor process is about 10.

[0006] In addition, most of the inductors are formed under the protection layer of a chip and near to the substrate, usually smaller than 10 μm. Therefore, in the application of the high-frequency devices the substrate becomes a conductor and consumes most of energy. Accordingly, the performance of the inductors deteriorates.

[0007] Although prior art proposed a three-dimensional structure comprising metal lines, vias and metal lines, the inductor is still too close to the substrate. Moreover, because of the process restriction, the via pattern cannot be formed as that of the metal lines and just forms a plurality of plugs between the metal lines. Therefore, the quality factor can be improved. Accordingly, lots of attention is paid in improving the quality factor and performance of inductors.

SUMMARY OF THE INVENTION

[0008] Therefore, an object of the present invention is to provide a method of fabricating an inductor which reduces the resistance of the inductor and improves the quality factor thereof without additional processes.

[0009] Another object of the present invention is to provide an inductor which is more distant from a substrate for reducing the interference resulting therefrom and improving efficacy of the chip.

[0010] The other object of the present invention is to provide an inductor having a multi-layer structure and a uniform thickness for enhancing the quality factor thereof.

[0011] The present invention discloses a method of fabricating an inductor formed on a substrate having at least one first dielectric layer thereon, the method comprising: forming a patterned first metal layer and a first inductor pattern within the first dielectric layer; forming a patterned second dielectric layer on the first dielectric layer for covering the first metal layer, the first inductor pattern and the first dielectric layer, the second dielectric layer having pluralities of first openings and second openings, wherein the first openings expose the first metal layer and the second openings expose the first inductor pattern; filling a metal within the first openings and the second openings for forming a second metal layer within the first openings and a second inductor pattern within the second openings, wherein the second metal layer electrically connects with the first metal layer and the second inductor pattern electrically connects with the first inductor pattern; and forming a patterned third metal layer on the second metal layer and a third inductor pattern on the second inductor pattern, wherein the third metal layer electrically connects with the second metal layer, the third inductor pattern electrically connects with the second inductor pattern, and the first inductor pattern, the second inductor pattern is similar to the third inductor pattern.

[0012] From the method described above, the present invention uses the multi-layer inductor pattern structure for increasing the thickness of the inductor. Therefore,

the resistance of the inductor is reduced and the quality factor is increased. Moreover, the present invention is simply to fabricate the inductor without additional processes.

[0013] The present invention discloses an inductor having at least one planarized dielectric layer thereon, which comprises: a first inductor pattern, a second inductor pattern and a third inductor pattern, wherein the first inductor pattern is formed within the dielectric layer, the second inductor pattern is formed on the first inductor pattern and electrically connecting therewith and the third inductor pattern is formed on the second inductor pattern and electrically connecting therewith. The first inductor pattern, the second inductor pattern is similar to the third inductor pattern.

[0014] From the method and the structure described above, the first inductor pattern, the second inductor pattern and the third inductor pattern are simultaneously from with the upmost metal layer, metal plugs and metal pads, respectively.

[0015] In the method and the structure described above, the first inductor pattern, the second inductor pattern and the third inductor pattern constitute a three-dimensional inductor structure. As to a symmetric inductor, the inductor has an overlapping area. In order to avoid shortage within the inductor, the first inductor pattern does not connect with the third inductor pattern via the second inductor pattern at the overlapping area.

[0016] The present invention also discloses another method of fabricating an inductor formed on a substrate having at least one first dielectric layer thereon, the method comprising: forming a patterned first metal layer and a first inductor pattern within the first dielectric layer; forming a patterned second dielectric layer on the first dielectric layer for covering the first metal layer, the first inductor pattern and the first dielectric layer, the second dielectric layer having pluralities of first openings and second openings, wherein the first openings expose the first metal layer and the second

openings expose the first inductor pattern; and forming a second metal layer filling the first openings and on the second dielectric layer and forming a second inductor pattern filling the second openings and on the second dielectric layer, wherein the second metal layer electrically connects with the first metal layer and the second inductor pattern electrically connects with the first inductor pattern.

[0017] From the method described above, the first inductor pattern, the second inductor pattern and the third inductor pattern are simultaneously formed with the upmost metal layer, metal plugs and metal pads, respectively. The metal plugs and metal pads are formed by the same deposition, lithography and etching processes.

[0018] In the method described above, the first inductor pattern and the second inductor pattern constitute a three-dimensional inductor structure. As to a symmetric inductor, the inductor has an overlapping area. In order to avoid shortage within the inductor, the first inductor pattern does not connect with the second inductor pattern at the overlapping area.

[0019] From the method and the structure described above, the present invention uses a multi-layer inductor pattern structure to increase the thickness of the metal wire, to reduce the resistance of the inductor, to enhance the quality factor and to improve the quality of the inductor.

[0020] In addition, each layer of the multi-layer inductor pattern structure of the present invention has similar pattern; therefore, the inductor has a uniform thickness and enhances the quality factor.

[0021] Additionally, the inductor and the metals pads can be formed together, which is more distant from the substrate than the prior art inductor; therefore, the

interference resulting from the substrate to the inductor can be reduced and the chip performance is improved.

[0022] Moreover, the process is simplified because the metal plugs and metal pads are formed by the same deposition, lithography and etching processes.

[0023] Furthermore, because the inductors with respect to the metal plugs and metal pads have the same material, the contact resistance resulting from application of different materials can be avoided and the quality factor of the inductor is improved.

[0024] In order to make the aforementioned and other objects, features and advantages of the present invention understandable, preferred embodiments accompanied with figures are described in detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] FIG. 1 is a schematic top view showing a first exemplary inductor of the present invention.

[0026] FIGS. 2A-2C are schematic cross-sectional views showing the structure along I-I' of FIG. 1.

[0027] FIGS. 3A-3C are schematic cross-sectional views showing the structure along II-II' of FIG. 1.

[0028] FIGS. 4A-4C are schematic top views showing the inductor patterns of FIG. 1.

[0029] FIG. 5 is a schematic top view showing a second exemplary inductor of the present invention.

[0030] FIGS. 6A-6C are schematic cross-sectional views showing the structure along III-III' of FIG. 5.

[0031] FIGS. 7A-7C are schematic top views showing the inductor patterns of FIG. 5.

DESCRIPTION OF SOME EMBODIMENTS

[0032] FIG. 1 is a schematic top view showing a first exemplary inductor of the present invention. FIGS. 2A-2C are schematic cross-sectional views showing the structure along I-I' of FIG. 1. FIGS. 3A-3C are schematic cross-sectional views showing the structure along II-II' of FIG. 1. Areas 101, 103 and 105 shown in FIG.1 correspond to those shown in FIGS. 2A-2C and FIGS. 3A-3C. In the embodiment, it is a symmetric circular-spiral inductor having an overlapping area.

[0033] Referring to FIGS. 1, 2A and 3A, the method of fabricating the inductor comprises first providing a substrate 100 having at least dielectric layer 102 thereon, which can be, for example, silicon oxide, silicon nitride or low-k material and can be formed, for example, by depositing the dielectric layer 102 on the substrate 100 and planarizing the dielectric layer 102 by chemical mechanical polishing (CMP). One of ordinary skill in the art will know that the dielectric layer 102 can be a multi-layer structure and that a plurality of devices and interconnects can be formed within the dielectric layer 102 and on the substrate 100.

[0034] A patterned metal layer 104a and an inductor pattern 104b are then formed within the dielectric layer 102, wherein the top view of the inductor pattern 104b is shown as FIG. 4A. The metal layer 104a is, for example, the upmost metal layer of the multi-layer interconnect structure on the substrate 100. It means that the inductor pattern 104b and the interconnect structure can be formed together during the same process.

[0035] Additionally, the material of the patterned metal layer 104a and an inductor pattern 104b is, for example, copper and formed, for example, by a damascene process. First, openings (not shown) are formed within the dielectric layer 102. Metal is then filled therein for forming the patterned metal layer 104a and an inductor pattern 104b.

[0036] Referring to FIGS. 1, 2B and 3B, a patterned dielectric layer 106 is formed on the dielectric layer 102 for covering the metal layer 104a, the inductor pattern 104b and the dielectric layer 102. In addition, the dielectric layer 106 has pluralities openings 108a and 108b, wherein the openings 108a expose the metal layer 104a and the openings 108b expose the inductor pattern 104b.

[0037] Additionally, the method of forming the dielectric 106 is, for example, by forming a dielectric layer (not shown) for covering the metal layer 104a, the inductor pattern 104b and the dielectric layer 102. Then, the dielectric layer 106 is planarized by CMP. The pattern of the dielectric layer is defined by lithography and etching processes for forming the openings 108a and 108b therein.

[0038] It should be noted that in order to avoid shortage of the inductor, openings 108b are not formed in areas 101 and 103 when they are formed within the dielectric layer 106. It means that the top inductor pattern (not shown) does not contact the inductor pattern 104b in areas 101 and 103 through the middle inductor pattern (not shown). Except of the areas 101 and 103, the contour of the openings 108b is similar to the inductor pattern 104b.

[0039] Referring to FIGS. 1, 2B and 3B, metal is filled in the openings 108a and 108b for forming a metal layer 110a within the openings 108a and an inductor pattern

110b within the openings 108b, wherein the metal layer 110a serves, for example, as metal plugs and electrically connects with the metal layer 104a.

[0040] In addition, the method of forming the inductor pattern 110b and the metal layer 110a is, for example, by forming a metal layer (not shown), which is, for example, tungsten and formed, for example, by low-pressure chemical vapor deposition (LPCVD) or sputtering. Then, planarization is performed for removing portions of metal outside the openings 108a and 108b. The metal layer 110a and the inductor pattern 110b therefore are formed. Accordingly, the metal layer 110a and the inductor pattern 110b are formed in the same process.

[0041] Moreover, the inductor 110b shown in FIG. 4B electrically connects with the inductor pattern 104b. In order to avoid the shortage of the inductor, the inductor pattern 110b are not formed in areas 101, 103 and 105 and the except inductor pattern 110b is similar to the inductor pattern 104b.

[0042] Referring to FIGS. 1, 2C and 3C, a patterned metal layer 112a is formed on the metal layer 110a and an inductor pattern 112b is formed on the inductor pattern 110b, wherein the metal layer 112a serves, for example, as metal pads and electrically connects with the metal layer 110a.

[0043] In addition, the metal layer 112a and the inductor pattern 112b are, for example, aluminum. The method is, for example, by forming a metal layer (not shown) on the dielectric layer 106, which is, for example, formed, by physical vapor deposition (PVD). Then, lithography and etching processes are performed for forming the metal layer 112a and the inductor pattern 112b. Accordingly, the metal layer 112a and the inductor pattern 112b therefore are formed in the same process.

[0044] Moreover, the inductor 112b shown in FIG. 4C electrically connects with the inductor pattern 110b. In order to avoid the shortage of the inductor, the inductor pattern 112b are only formed at areas 103 and 105 and the except inductor patterns 112b, 110b and 104b have similar pattern.

[0045] It should be noted that the inductor patterns 112b, 110b and 104b constitute a three-dimensional inductor structure as shown in FIG. 1 and forms an overlapping area 105. The inductor pattern 104b does not connect with the inductor pattern 112b via the inductor pattern 110b at the overlapping area 105. By the layout of the overlapping of the three-dimensional inductor structure, a current only flows along the first inductor pattern when the current first time flows through the overlapping area and the current only flows along the third inductor pattern when the current second time flows through the overlapping area. The shortage of the inductor at the overlapping area can be avoided.

[0046] Additionally, the present invention is not limited to steps described above. The metal layers 110a and 112a and the inductor patterns 110b and 112b can be formed by dual-damascene process.

[0047] From the method described above, the present invention uses a multi-layer inductor pattern structure to increase the thickness of the metal wire, to reduce the resistance of the inductor, to enhance the quality factor and to improve the quality of the inductor. Moreover, no extra process is required in the present invention.

[0048] In the method of the present invention, the openings 108b of the inductor pattern 110b can be formed with the openings 108a simultaneously. Because the openings 108a and 108b are at the top layer of the interconnect structure, the process restriction is reduced and the openings 108b is similar to the inductor 104b.

[0049] Following are the descriptions of the inductor formed from the method described above. Referring to FIGS. 1, 2C and 3C, wherein FIG. 1 is a schematic top view showing a first exemplary inductor of the present invention, FIG. 2C is a schematic cross-sectional view showing the structure along I-I' of FIG. 1 and FIG. 3C is a schematic cross-sectional view showing the structure along II-II' of FIG. 1. Areas 101, 103 and 105 shown in FIG.1 correspond to those shown in FIGS. 2C and 3C. Area 105 represents the overlapping of the areas 101 and 103.

[0050] The inductor of the present invention is formed on a substrate 100 having at least one dielectric layer 102 thereon. The inductor comprises three inductor patterns 104b, 110b and 112b.

[0051] The inductor pattern 104b is formed on the dielectric layer 102 as shown in FIG. 4A. The metal layer 104a is also formed therein. It means that the inductor pattern 104b and the metal layer 104a are formed within the same dielectric layer. The metal layer 104a is, for example, the upmost metal layer of the multi-layer interconnect structure on the substrate 100. The material of the inductor pattern 104b and the metal layer 104a are, for example, copper. It should be noted that the inductor pattern 104b is only formed at the overlapping area 105 of the areas 101 and 103.

[0052] The inductor pattern 110b is formed on the pattern inductor 104b as shown in FIG. 4B. Except of the overlapping area, the inductor patterns 110b and 104b have similar pattern and electrically connect to each other. The metal layer 110a is formed on the metal layer 104a which means that the metal layer 110a and the inductor pattern 110b are formed within the same layer. The metal layer 110a is, for example, metal plugs. The material of the metal layer 110a and the inductor pattern 110b are, for

example, tungsten. It should be noted that the inductor pattern 110b is not formed at the areas 101 and 103 including the area 105.

[0053] In addition, the inductor pattern 112b is formed on the pattern inductor 110b as shown in FIG. 4C. Except of the overlapping area, the inductor patterns 112b, 110b and 104b have similar pattern and the inductor patterns 112b and 110b electrically connect to each other. The metal layer 112a is formed on the metal layer 110a which means that the metal layer 112a and the inductor pattern 112b are formed within the same layer. The metal layer 112a is, for example, metal pads. It should be noted that the inductor pattern 112b is only formed at the overlapping are 105 of the areas 101 and 103.

[0054] Additionally, the inductor patterns 104b, 110b and 112b constitute a three-dimensional inductor structure as shown in FIG. 1. The overlapping area 105 of the three-dimensional inductor structure is composed of the inductor patterns 104b, 110b and 112b. The inductor pattern 104b does not connect with the inductor pattern 112b via the inductor pattern 110b at the overlapping area 105. The shortage of the inductor at the overlapping area can be avoided.

[0055] FIG. 5 is a schematic top view showing a second exemplary inductor of the present invention. FIGS. 6A-6C are schematic cross-sectional views showing the structure along III-III' of FIG. 5. In the embodiment, it is a concentric circular-spiral inductor.

[0056] Referring to FIGS. 5 and 6A, the method of fabricating the inductor comprises first providing a substrate 200 having at least dielectric layer 202 thereon, which can be, for example, silicon oxide, silicon nitride or low-k material and can be formed, for example, by depositing the dielectric layer 202 on the substrate 200 and

planarizing the dielectric layer 202 by chemical mechanical polishing (CMP). One of ordinary skill in the art will know that the dielectric layer 202 can be a multi-layer structure and that a plurality of devices and interconnects can be formed within the dielectric layer 202 and on the substrate 200.

[0057] A patterned metal layer 204a and an inductor pattern 204b are then formed within the dielectric layer 202, wherein the top view of the inductor pattern 204b is shown as FIG. 7A. The metal layer 204a is, for example, the upmost metal layer of the multi-layer interconnect structure on the substrate 200. It means that the inductor pattern 204b and the interconnect structure can be formed together during the same process.

[0058] Additionally, the material of the patterned metal layer 204a and an inductor pattern 204b is, for example, copper and formed, for example, by a damascene process. First, openings (not shown) are formed within the dielectric layer 202. Metal is then filled therein for forming the patterned metal layer 204a and an inductor pattern 204b.

[0059] Referring to FIGS. 5 and 6B, a patterned dielectric layer 206 is formed on the dielectric layer 202 for covering the metal layer 204a, the inductor pattern 204b and the dielectric layer 202. In addition, the dielectric layer 206 has pluralities openings 208a and 208b, wherein the openings 208a expose the metal layer 204a and the openings 208b expose the inductor pattern 204b. The contour of the openings 208b is similar to the inductor pattern 204b, which means the openings 208b are formed along the inductor pattern 204b.

[0060] Additionally, the method of forming the dielectric 206 is, for example, by forming a dielectric layer (not shown) for covering the metal layer 204, the inductor

pattern 104b and the dielectric layer 202. Then, the dielectric layer 206 is planarized by CMP. The pattern of the dielectric layer is defined by lithography and etching processes for forming the openings 208a and 208b therein.

[0061] Referring to FIGS. 5 and 6C, the metal layer 210a of the openings 208a and 208b and an inductor pattern 210b are formed within the dielectric layer 206, wherein the metal layer 110a electrically connects with the metal layer 204a which can be deemed being composed of the metal layer 212a and the metal layer 214a. The metal layer 212a of the openings 208a serves, for example, as metal plugs and the metal layer 214a on the dielectric layer 206 serves, for example, as metal pads.

[0062] The inductor pattern can be deemed as a single inductor pattern or be composed of the inductor pattern 212b of the openings 208b and the inductor pattern 214b on the dielectric layer 206 as described in first embodiment. Because the openings 208b has similar pattern as that of the inductor pattern 204b, the inductor patterns 212b, 214b and 204b have similar pattern.

[0063] In addition, the metal layer 210a and the inductor pattern 210b are, for example, aluminum. The method is, for example, by forming a metal layer (not shown) on the dielectric layer 206, which is, for example, formed, by physical vapor deposition (PVD). Then, lithography and etching processes are performed for forming the metal layer 210a (212a and 214a) and the inductor pattern 210b (212b and 214b). Accordingly, the metal layer 210a and the inductor pattern 210b therefore are formed in the same process.

[0064] Similarly, the present invention uses a multi-layer inductor pattern structure to increase the thickness of the metal wire, to reduce the resistance of the

inductor, to enhance the quality factor and to improve the quality of the inductor. Moreover, no extra process is required in the present invention.

[0065] In the method of the present invention, the openings 208b of the inductor pattern 210b can be formed with the openings 208a simultaneously. Because the openings 208a and 208b are at the top layer of the interconnect structure, the process restriction is reduced and the openings 208b and the inductor 204b have similar pattern.

[0066] Moreover, in the embodiment the metal layers 212a and 214a and the inductor patterns 212b and 214b can be formed during the same deposition, lithography and etching processes; therefore, this embodiment is more simplified than the first embodiment. In addition, because the inductor patterns 212b and 214b have the same material, the contact resistance thereof is reduced and quality factor is enhanced. Moreover, the inductor pattern 212b can be aluminum. Compared with tungsten used in the first embodiment, the contact resistance thereof is reduced and quality factor is enhanced.

[0067] Following are the descriptions of the inductor formed from the method described above. Referring to FIGS. 5 and 6C, wherein FIG. 5 is a schematic top view showing a first exemplary inductor of the present invention and FIG. 6C is a schematic cross-sectional view showing the structure along III-III' of FIG. 5.

[0068] The inductor of the present invention is formed on a substrate 200 having at least one dielectric layer 202 thereon. The inductor comprises three inductor patterns 204b and 210b.

[0069] The inductor pattern 204b is formed on the dielectric layer 202 as shown in FIG. 7A. The metal layer 204a is also formed therein. It means that the inductor pattern 204b and the metal layer 204a are formed within the same dielectric layer. The

metal layer 204a is, for example, the upmost metal layer of the multi-layer interconnect structure on the substrate 200. The material of the inductor pattern 204b and the metal layer 204a are, for example, copper.

[0070] In addition, the inductor pattern 210b is formed on the pattern inductor 204b as shown in FIG. 7C. The inductor patterns 210b and 204b connect to each other. Additionally, the metal layer 210a is formed on the metal layer 204a which is formed within the same layer of the inductor pattern 210b. In the embodiment, the inductor pattern 210b can be deemed being composed of the inductor patterns 212b shown in FIG. 7B and 214b shown in FIG. 7C. Similarly, the metal layer 212a can be deemed as being composed of the metal layers 212a and 214a. The metal layer 212a of the openings 208a serves, for example, as metal plugs and the metal layer 214a on the dielectric layer 206 serves, for example, as metal pads. The material of the metal layer 210a and inductor pattern 210b can be, for example, aluminum.

[0071] Of course, the layout of the inductor is not limited to the symmetric circular-spiral type shown in FIG. 1 or concentric circular-spiral type shown in FIG. 5. The other type inductor, such as a symmetric rectangular-spiral type or a concentric rectangular-spiral type, can also be applied to the present invention.

[0072] Moreover, in the symmetric circular-spiral inductor of the first embodiment the first, second and third inductor patterns are formed by different deposition processes. However, the present invention is not limited thereto. In the inductor of the first embodiment, the second and third inductor patterns can be formed during the same deposition, lithography and etching processes as those of the second embodiment. In other words, any type of inductor can be formed by the method of the first embodiment or the second embodiment.

[0073] Accordingly, the present invention uses a multi-layer inductor pattern structure to increase the thickness of the metal wire, to reduce the resistance of the inductor, to enhance the quality factor and to improve the quality of the inductor.

[0074] Moreover, each layer of the multi-layer inductor structure of the present invention has similar pattern for forming a uniform thickness thereof and enhancing the quality factor.

[0075] Furthermore, the inductor and the metals pads can be formed together, which is more distant from the substrate than the prior art inductor; therefore, the interference resulting from the substrate to the inductor can be reduced and the chip performance is improved.

[0076] Moreover, the process is simplified because the metal plugs and metal pads are formed by the same deposition, lithography and etching processes.

[0077] Furthermore, because the inductors with respect to the metal plugs and metal pads have the same material, the contact resistance resulting from application of different materials can be avoided and the quality factor of the inductor is improved.

[0078] Although the present invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be constructed broadly to include other variants and embodiments of the invention which may be made by those skilled in the field of this art without departing from the scope and range of equivalents of the invention.